Distributed sensing, damage detection and analysis in FRP uni-directional composites

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ABSTRACT
The highly dispersive, attenuating, heterogeneous and anisotropic nature of unidirectional fiber reinforced polymer matrix (FRP) composites places an emphasis on high density local sensing as opposed to lower density more-global sensing strategies.

This thus requires a relatively high density of sensors for damage characterization and detection, which naturally implies large quantities of data requiring substantial bandwidth and processing power.

Distributing processing with the sensors themselves results in a decreased demand for bandwidth and lower computational power needed at each node in what is now a distributed processing computer. Desired information, time constraints and mechanical considerations place both hard and soft constraints on our network helping to define its architecture. I will present investigated computing architectures – their benefits and limitations – as they relate to the various constraints involved, as well as our progress in damage assessment with the distributed sensing network.

1. CONSTRAINTS

1.1 Unidirectional Fiber Reinforced Polymer Composites

Our goal is to embed network of sensors and processing elements (PEs) in a glass fiber reinforced polymer matrix composite. That being said, the network and sensors should be significantly smaller than the composite we are embedding it in, or else we just have a resin covered circuit board. Size of the electronics is also important since the discontinuities of their mechanical properties with that of the FRP composite creates stress localizations, lower bonding strengths and lower fatigue life, all of which is exacerbated by larger and increased numbers of inclusions.

The heterogeneous anisotropic nature of the unidirectional FRP composite causes significant attenuation and dispersion of acoustic waves especially in propagation directions with an orthogonal component to the fiber direction. Wave speed is also very directionally dependant with a factor of 2 difference between 0° and 90° with respect to the fiber direction (see Figure 1).

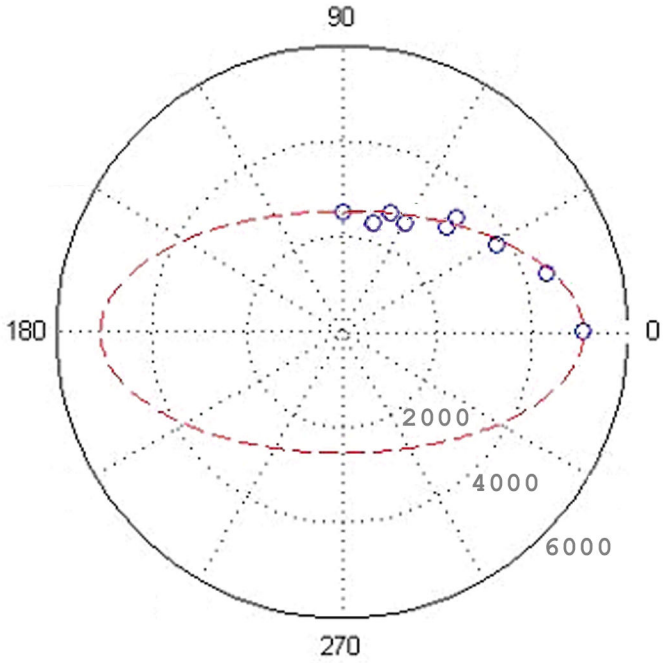

Figure 1. Acoustic wave velocity (m/s) measured in unidirectional FRP plate – made using pencil graphite break test and collinear ultrasonic transducers.

These complications make a case for a relatively dense network of sensors to sufficiently pick up matrix cracking signals without extensive signal amplification and noise reduction techniques. Of course, one must balance real the estate demands of signal conditioning electronics against those of the sensor and processing element. This paper is not to address this balance and really makes the assumption that next-generation microcontrollers will address these issues with higher integration and smaller sizes.

1.2 Current Generation Electronics

We would love to use next generation electronics and sensors in our project. The only problem is that – despite what marketing departments would have us believe – we only have access to current generation and older products.

1.2.1 SiLabs® C8051F300 MCU

Our current processor of choice is the Silicon Laboratories® (previously Cygnal) C8051F300 microcontroller. The combination of its form factor – 3x3 mm 11-pin MLP – and its capabilities made it our processor of choice for the time being. Table 1 outlines its capabilities.

Table 1. SiLabs® C8051F300 microcontroller information and features [1]

Package	Throughput	Memory		Analog Peripherals		Digital Peripherals			
		RAM	Flash	ADC	Comparator	I/O	Serial Ports	PCA	Timers
3x3 mm, 11-pin MLP	25 MIPS @ 24.5 MHz	256 bytes	8k, in-system programmable	8-bit, 500ksps	0.4 μA Curr, 100 mV Diff, 100 ns RT	8-port	SMBus, UART	16-bit	3 general purpose Timers

1.2.2 Future Expectations

As newer technologies emerge, the cutting edge tends to become cheaper and thus more feasible for manufacturers whose market share is not entirely dependant on being at the bleeding edge. This is especially true in photolithography for the semiconductor industry. Giants such as Intel, AMD, and IBM are using 65 and 45 nm processes, since their primary goal has been increased speed through miniaturization. While speed is important to any manufacturer of ICs, capabilities and other performance metrics such as power consumption are just as strong as driving forces. However, as the giants move on to the latest and greatest, smaller players get a

piece of the old cutting edge. Additionally, consumer demand for mobile phones and personal media players is pushing manufactures to put their devices in smaller and smaller packages. In the end, while our 8051 microcontroller is probably fabricated using a feature size of 0.130 um or larger, a switch to cutting edge technologies would allow our microcontroller to occupy at least $1/9^{th}$ their current area. In general, however, an expanded feature set is produced while shrinking the size of the component less. These microcontrollers are only getting smaller and more powerful with more memory and a greater feature set, all of which makes them more applicable to our application.

2. NETWORK ARCHITECTURES

While there are an innumerable number of network configurations and designs possible, the following are only the networks which we are currently investigating, presented in order of complexity. The reasons for their inclusion into our investigation will be outlined in the following sections. For now, it should suffice to say that our self imposed hardware limitations as well as a desire to optimize, limit complexity and limit components were the factors driving our decisions.

2.1 Global Bus Network

The global bus network (Figure 2) is quite simply several sensor nodes or processing elements (PEs) connected by a single bus. The geometrical arrangement of the bus is inconsequential to its performance or viability. The four-by-four array shown in Figure 2 is used for simplicity of comparison with future networks as well as to support the assumption of composite panel coverage. The bus itself can likewise be configured in any given way, but is portrayed linearly for simplicity.

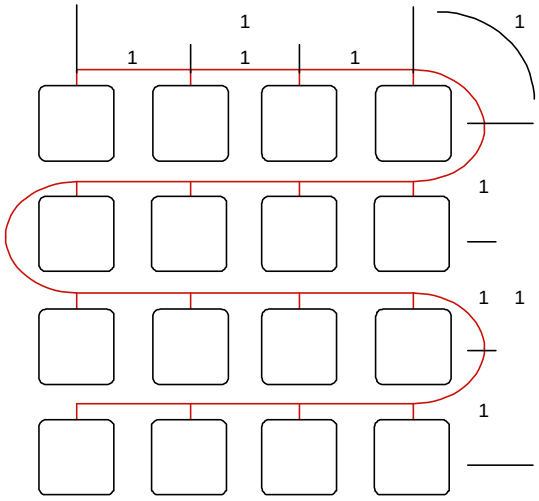

Figure 2. Global Bus network. Similar to the mesh network in that all PEs are peers, but each PE is connected to every other PE via a common bus, as opposed to individual connections. The numbers in the figure represent the network distance between two PEs. Nearest neighbors are at a distance of 1 as are the two PEs in the same at opposite ends of a row or a column. The number in the upper right indicates the network distance between the PEs at (1,1) and (4,4); in this case it is also 1.

The advantages of this network lay in its simplicity. Use of a single bus network means less communications protocols and programming space required in the limited 8k memory. Additionally, having only one serial port means fewer interrupts increasing the probability of fast response times to sensor acquired stimulus as well as reducing demand for computational time – interrupts and their returns are some of the most expensive computational sequences for our 8051 microcontroller.

As previously stated, we are currently focusing our research efforts on acoustic emissions. While it is interesting to make spatial comparisons of AE metrics, the generally performed analysis is more analogous to temporal as opposed to spatial delineations in acoustic activity – with the exception of special detection. We can then assume that with each PE collecting data from an equal set of sensors, the network memory load would be roughly balanced. Further, since each PE has most of the data it needs to make its evaluation, little to no communication

is necessary to redistribute data. Finally, if each PE is collecting the same kind of data, each should be performing the same task and the processing load should be roughly balanced as well. This leaves little communication necessary on the network except for some occasional administration such as polling and synchronization. Thus a distributed network connected by a single bus is our network of choice for initial embedding. Tests of this network in practice are on going but look promising.

This network design has its draw backs. These are primarily due to communications latency due to an inability to communicate in parallel. Due to this limitation, location detection is currently done quite crudely via first arrival techniques – the first sensor to sense the AE or failure is the assumed location of the AE or failure. Image processing techniques perform miserably if at all, and would perform better on a multi-bus system such as the row-column array network, but that is left for future investigation.

2.2 Nearest Neighbor Mesh

At the beginning of our investigation we had little idea what our sensing strategy would be and thus determining a specific network was somewhat arbitrary. This left us wanting to design a network that was robust and minimally fault tolerant and would work well with edge finding algorithms. When combined with the notion that as little electronics as possible should be embedded and that all sensors should be of peer status, we thought that the nearest-neighbor mesh (NN mesh – see Figure 3) implementation would be an appropriate starting point.

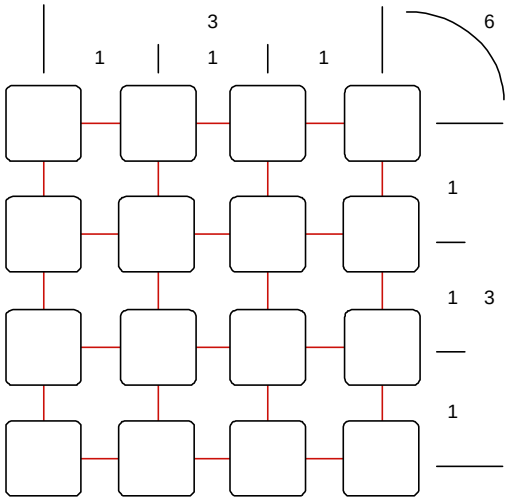

Figure 3. Nearest-neighbor mesh network. A PE's communication is restricted to its neast neighbors only. For communication with other nodes, a message passing protocol must be developed. The numbers represent the effective network distance, thus to pass a message from the PE in the upper left to the PE in the bottom right takes 6 steps. This newtwork can easily be improved by connecting the first and last PE in each row and column making it a torus network.

In this implementation a given processing element can only communicate with its immediate neighbors, requiring directional communication isolation. Being limited on hardware implemented communications (only two while we have four neighbors), entire software protocols were written. These all required strict synchronization across the network, a requirement which can be problematic especially with large network distances.

Additionally, these protocols required rerouting algorithms in the case of halting and receive omission at an intermediary PE. This was designed to allow messages to arrive at their destination so long as network partition had not occurred – see Figure 4.

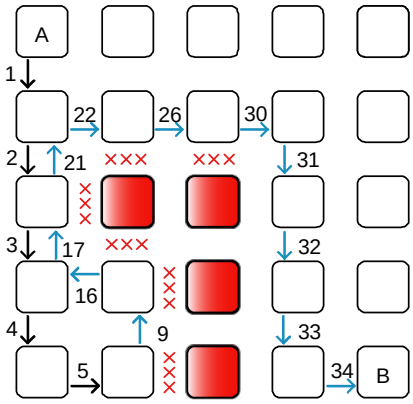

Figure 4. Example of developed message routing algorithm for our nearest neighbor mesh network.

The major problems with the NN mesh network were latency, synchronization and scalability. Latency was improved by shifting the network to a torus design and allowing communication to only flow in a single direction along any given column or row. This has the additional benefit of allowing the TX and RX UART pins to handle opposite directions reducing communications costs – if only there were two UARTS. By having alternating communication directions in the neighboring rows and columns, message delivery would still be highly probably, but no longer guaranteed. All workarounds to overcome many of the deficiencies of the C8051F300 in the nearest neighbor mesh structure usually involved higher overhead adding significantly to the code space governing communication protocol and message passing.

2.3 Row-Column Bus Array

A compromise between the global bus and the nearest neighbor mesh can be found in the row-column bus array (Figure 5). It manages to keep any given network distance down to 2 communications while allowing for simultaneous communications to occur. This also fits nicely into our C8051F300 paradigm as a 9-bit UART protocol can be used for columns while the SMBus is used for row communications. This leaves little additional protocol work with the exception of message passing, receive omission checking, etc – generally much less complex than the NN mesh network discussed in section 2.2 and can be run in asynchronous mode. The code space dedicated to communications is much less than the mesh and strict synchronization is not necessary (though easier to perform).

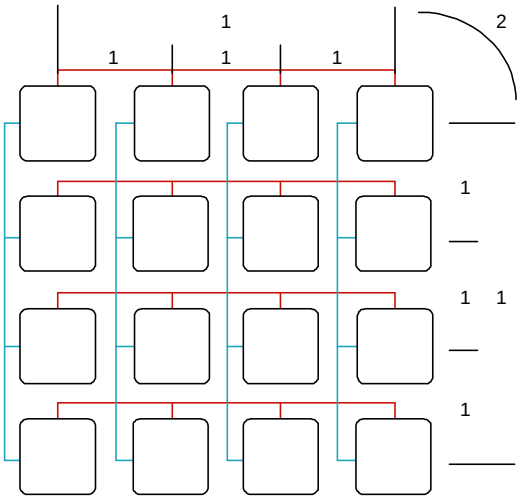

Figure 5. Row-Column Bus Array. Each row and column has its own bus to pass data. This significantly speeds up average communication over global bus network (Figure 2) by allowing simultaneous communications over the network while only increasing the network distance to 2.

2.4 4-Tree

Due to the latency and timing issues of the NN mesh network and after viewing dismal performance of the FFT [2] in our non-torus implementation we began work on the 4-tree network – the 2-D representation of which is shown in Figure 6. While achieving significant improvement with hierarchical compatible algorithms such as the FFT [3], we also achieved a scalability that was previously prohibitively expensive in regards to latency. In the tree network, communications times increased as $\log_2$ of the network size.

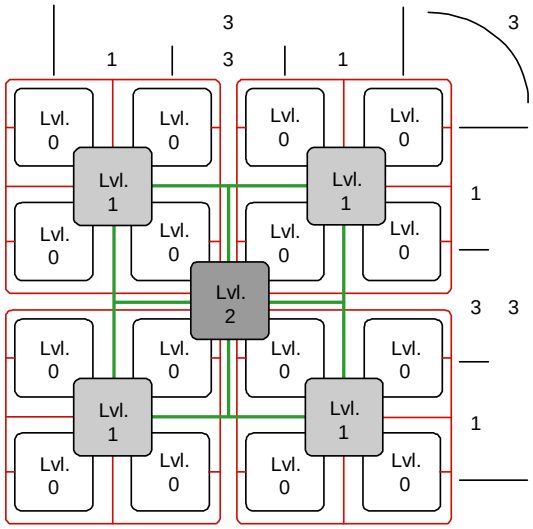

Figure 6. 4-Tree Network. In this implementation of a tree, each node – minus the root (Lvl. 2) – has a parent and three siblings. As implemented here, a bus is shared among siblings of the same parent, allowing direct communication with one another. Communication with a "cousin" is performed via message passing through parent nodes. The pyramid network is related to the tree, but allows communication amongst peers in the network with out parents acting as intermediaries – a combination of the mesh and tree networks.

The disadvantages were the extra number of PEs required due to the hierarchy scheme – increasing power consumption while decreasing mechanical integrity. The inefficiency of implementing edge finding algorithms, which require data from ones nearest-neighbors only is also a disadvantage (they still occurred slightly faster than the NN mesh, but required more memory to implement). More total memory is also required to implement algorithms on the 4-Tree network. As a percentage of total memory, it is less than that of the NN mesh of the RC bus network and the distribution of memory consumption is beneficial for sensing and algorithmic strategies. Specifically, the lowest level PEs whose primary job is to capture data and perform basic analysis are required to use less of their memory for communications and algorithmic implementations than the higher levels.

There is also a modified Tree Network – the pyramid network – which is essentially a combination of the tree and the NN mesh networks. While this helps with the efficiency of algorithms that are benefited by easy data passing between same level PEs, it greatly increases development of communications and general network connectivity. The lack of hardware implemented communications in our microcontroller of choice – only 1 UART and 1 SMBus – make realization of a pyramid network challenging but is something we have begun investigating with larger more fully loaded microcontrollers.

3. PROGRESS AND PLANS

While we have currently developed the above networks, our current focus is on the simplest of them, the global bus network. For all the reasons listed in its section we feel it is a good starting point for actual embedding and monitoring hits in UTS and tensile-tensile fatigue tests. We have begun tensile tests with sensors connected to an external network. This is a progression of our extensive mechanical fidelity tests an modeling in both bending [4] and tensile [5] quasi-static and fatigue tests.

4. ACKNOWLEDGEMENTS
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[1] Silcon Laboratories, "C8051F300_short",http://www.silabs.com/public/documents/tpub_doc/dshort/Microcontrollers/Small_Form_Factor/en/C8051F300_Short.pdf, 2005

[2] Loewke, K., Meyer, D., Starr, A., Nemat-Nasser, S. "Signal identification in smart composite materials using the two-dimensional fast fourier transform", *Smart Mater. Struct.* **14** [895–903](2005)

[3] Rye, P., "Embedded microcontroller networks: Acoustic materials health monitoring," *Proc. of SPIE* **6530** (2007)

[4] Schaaf, K., Rye, P., Nemat-Nasser, S. "Optimization studies of self-sensing composites," *Proc. Of SPIE* **6529** (2007)

[5] Ghezzo, F., Nemat-Nasser, S., "Effects of embedded SHM sensors on the structural integrity of glass fiber/epoxy laminates under in-plane loads." *Proc. of SPIE* **6530** (2007)